UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,009	07/20/2000	Kwang-Jin Yang	P56077	3128

8439 7590 11/02/2005

ROBERT E. BUSHNELL
1522 K STREET NW
SUITE 300
WASHINGTON, DC 20005-1202

EXAMINER	
CURS, NATHAN M	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,009	YANG ET AL.	
	Examiner	Art Unit	
	Nathan Curs	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8, 12, 13, 15-17, 19-36 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12,13,15,17,19-26,28,30-32,34,35 and 41-43* is/are rejected.

7)☒ Claim(s) *16, 27, 29 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 36 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 29. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17, 19-25, 28, 30-32, 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Banwell et al. (US Patent No. 6285722).

Regarding claim 17, Mokhtari et al. disclose a method of operating a receiver which functions independently of a bit rate of a received signal, comprising: receiving an original signal (fig. 2, Data IN signal); generating a resultant signal by performing an exclusive-OR operation on a first signal and a second signal, said first signal comprising said original signal delayed by a predetermined quantity of time, said second signal comprising said original signal not delayed

(fig. 5 and page 509, col. 2, paragraph 1); determining a bit rate of said original signal by low-pass filtering said resultant signal, and determining a voltage level of the low-pass filtered resultant signal (fig. 6 and page 509, col. 2, paragraph 3); generating a reference clock signal separate from said original signal and in dependence upon said determined bit rate (fig. 3, element Clock Out); and recovering an input clock signal and data from said original signal in dependence upon said reference clock signal (figs, 3 and 4, element Decision Circuit). Mokhtari et al. do not disclose deriving a bit rate of the original signal directly from a voltage level of the low-pass filtered signal without using a phase locked loop. Banwell et al. disclose an apparatus for variable bit rate clock recovery (figs. 3, 8 and 12a and col. 4, lines 35-59, col. 10, line 26 to col. 11, line 13), without using a phase-locked loop (col. 2, line 60 to col. 3, line 2, and col. 3, lines 23-30), where a bit rate is derived directly from a voltage of a low-pass filter of the clock recovery circuit (fig. 12a, element 1220 and fig. 8, elements 830 and RE). Further, the transition detector of Banwell et al. (fig. 3, element 320) is analogous to the edge detector of Moktari et al. (fig. 5). Based on the teaching of Banwell et al. regarding the disadvantages of a phase-locked loop variable bit rate clock recovery circuit, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the clock recovery circuit of Mokhtari et al., to remove the PLL of Moktari et al. and substitute the non-phase locked-loop clock recovery teaching of Banwell et al., in order to provide variable rate clock recovery that is not subject to the problem of locking to harmonics or sub-harmonics of the bit rate in systems with wide ranges of bit rates such as WDM systems.

Regarding claim 19, the combination of Mokhtari et al. and Banwell et al. discloses receiving an original signal comprising an input optical signal (Mokhtari et al.: page 508, col. 1, paragraphs 3 and 4; and col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (Mokhtari et al.: page 508, col. 2, paragraph

4); outputting two duplicate signals substantially equivalent to the electrical signal, the two duplicate signals comprising a primary signal and a secondary signal (Mokhtari et al.: fig. 5); and delaying the primary signal by the predetermined quantity of time (Mokhtari et al.: fig. 5 and page 509, col. 2, paragraph 1), and outputting a delayed primary signal comprising the first signal (Mokhtari et al.: fig. 5).

Regarding claim 20, the combination of Mokhtari et al. and Banwell et al. discloses a 3R regenerator with optoelectric conversion at the signal input (Mokhtari et al.: page 508, col. 2, paragraph 4), and disclose the first, and second signals (Mokhtari et al.: fig. 5), where these signals are inherently electrical for a 3R regenerator with optoelectric conversion.

Regarding claim 21 and 24, the combination of Mokhtari et al. and Banwell et al. discloses a method comprising receiving optical signals having a plurality of different bit rates (Mokhtari et al.: page 508, col. 1, paragraphs 3 and 4, and col. 2, paragraph 3).

Regarding claim 22, the combination of Mokhtari et al. and Banwell et al. discloses an original signal received comprising a plurality of original signals received (Mokhtari et al.: page 508, col. 1, paragraphs 3, 4, and 6), the recovering of the input clock signal and data from the original signal being performed for the plurality of original signals received (Mokhtari et al.: figs. 2 and 3 and Banwell et al.: fig. 3), the plurality of original signals received having a respective plurality of different bit rates (Mokhtari et al.: page 508, col. 1, paragraphs 3, 4, and 6).

Regarding claim 23, the combination of Mokhtari et al. and Banwell et al. discloses recovering of the input clock signal and data from the original signal performed for a plurality of original signals received (Mokhtari et al.: figs. 2 and 3 and Banwell et al.: fig. 3), the plurality of original signals received having a respective plurality of different bit rates (Mokhtari et al.: page 508, col. 1, paragraphs 3, 4 and 6).

Regarding claim 25, the combination of Mokhtari et al. and Banwell et al. discloses receiving an input optical signal (Mokhtari et al.: fig. 2, Data IN signal); converting said input optical signal to an original electrical signal (Mokhtari et al.: page 508, col. 2, paragraph 4); outputting two duplicate signals substantially equivalent to said original electrical signal, said two duplicate signals comprising a primary signal and a secondary signal (Mokhtari et al.: fig. 3, split signals from "data in"); and delaying said primary signal by said predetermined quantity of time, and outputting said primary signal, said delayed primary signal comprising said first signal, said outputted primary signal comprising said second signal (Mokhtari et al.: fig. 5, as illustrative of the edge detector of fig. 3).

Regarding claim 28, Mokhtari et al. disclose a 3R regenerator receiving an input optical signal (page 508, col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit for receiving an electrical signal (fig. 3, elements Edge Detector and PLL), where the edge detector and PLL comprise an identification unit, for generating a first signal comprising an electrical signal delayed by a predetermined quantity of time and for generating a second signal comprising an electrical signal not delayed (fig. 5), for forming a third signal by performing an exclusive-OR logic operation upon the first and second signals (fig. 5), and for detecting a bit rate in dependence upon the third signal and a clock generator for generating a reference clock signal in dependence upon the detected bit rate (fig. 3); and a recovery unit for recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3). Mokhtari et al. disclose that the identification unit comprises: a first unit for delaying the original electrical signal and for performing the exclusive-OR operation upon the first and second signals and for forming the third signal (fig. 5); and a second unit for filtering the third signal, and for detecting the bit rate in

dependence upon a voltage level of the filtered third signal (fig. 6 and page 509, col. 2, paragraph 4). Mokhtari et al. disclose the reference clock being branched to the decision circuit and to a clock output. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to output the recovered clock from the decision circuit, along with the recovered data, which modification at most would require simple, well known, inverter logic and another output from the decision circuit, in order to eliminate the need to branch the reference clock to the decision circuit and it's own separate output. Mokhtari et al. disclose a Reshaping/Limiting stage between the O/E converter and the identification unit, thus the electrical signal output from the O/E converter is the original signal, which passes through the disclosed Reshaping/Limiting stage before entering the identification unit. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that, given the reshaping function inherent to the decision circuit of the Retiming block of Mokhtari et al., the separate Reshaping/Limiting block as disclosed could be removed as being redundant depending on the degree of distortion of the incoming signal, since the Retiming block both reshapes and retimes. In the case where the Retiming block performs all reshaping and retiming functions, the original output signal from the O/E converter would go directing to the Retiming block. Mokhtari et al. do not disclose deriving a bit rate of the original signal directly from a voltage level of the low-pass filtered signal without using a phase locked loop. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Banwell et al. with Mokhtari et al. as described above for claim 17.

Regarding claim 30, the combination of Mokhtari et al. and Banwell et al. discloses an original signal received comprising a plurality of original signals received (Mokhtari et al.: page 508, col. 1, paragraphs 3, 4, and 6), the recovering of the input clock signal and data from the original signal being performed for the plurality of original signals received (Mokhtari et al.: page

509, col. 1, paragraphs 3 and 4), the plurality of original signals received having a respective plurality of different bit rates (Mokhtari et al.: page 508, col. 1, paragraphs 3, 4, and 6).

Regarding claim 31, the combination of Mokhtari et al. and Banwell et al. discloses an apparatus, comprising: a fiber optic system including electrical 3R regeneration (Mokhtari et al.: page 508, col. 1, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes an optoelectric converter to convert an input optical signal to an original electrical signal (Mokhtari et al.: page 508, col. 2, paragraph 4).

Regarding claim 32, the combination of Mokhtari et al. and Banwell et al. discloses an identification unit comprising a bit rate identification unit (Mokhtari et al.: fig. 5, and page 509, col. 2, paragraph 1 and Banwell et al.: fig. 3).

Regarding claim 42, the combination of Mokhtari et al. and Banwell et al. discloses that said recovery step is performed by a programmable recovery unit (Mokhtari et al.: fig. 3, where the variable-rate recovered clock, considering the applied teaching of Banwell et al. fig. 3, input to the decision circuit, makes the decision circuit a programmable recovery unit).

Regarding claim 43, Mokhtari et al. disclose that the recovery unit comprises a programmable recovery unit (Moktari et al.: fig. 3, where the variable-rate recovered clock, considering the applied teaching of Banwell et al. fig. 3, input to the decision circuit, makes the decision circuit a programmable recovery unit).

4. Claims 1-8, 12-13, 34 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511

vol. 2) in view of Banwell et al. (US Patent No. 6285722), and further in view of Ishihara (US Patent No. 5557648).

Regarding claim 1, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including an electrical 3R function (page 508, col. 2, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes a converter for converting an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit for receiving an electrical signal (fig. 3, elements Edge Detector and PLL), where the edge detector and PLL comprise an identification unit, for generating a first signal comprising an electrical signal delayed by a predetermined quantity of time and for generating a second signal comprising an electrical signal not delayed (fig. 5), for comparing the first and second signals and for forming a third signal in dependence upon the comparing of the first and second signals (fig. 5), and for detecting a bit rate in dependence upon the third signal (page 508, col. 1, paragraph 4 and fig. 3); a clock generator for generating a separate reference clock signal in dependence upon the detected bit rate (fig. 3) and a recovery unit for recovering data from the input optical signal in dependence upon the reference clock signal (fig. 3, element Decision Circuit); wherein said identification unit further comprises: a first unit for delaying said electrical signal, for performing an exclusive-OR operation upon said first and second signals, and for forming said third signal in dependence upon said exclusive-OR operation performed upon said first and second signals (fig. 5). Mokhtari et al. disclose a second unit comprising: a low-pass filter for filtering the third signal, and bit rate deriving unit for deriving the bit rate in dependence upon information related to a voltage level and a predetermined bit rate (fig. 6; and page 509, col. 2, paragraph 4). Mokhtari et al. disclose the reference clock being branched to the decision circuit and to a clock output. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to output the recovered clock from the decision circuit, along with the recovered data,

which modification at most would require simple, well known, inverter logic and another output from the decision circuit, in order to eliminate the need to branch the reference clock to the decision circuit and it's own separate output. Mokhtari et al. disclose a Reshaping/Limiting stage between the O/E converter and the identification unit, thus the electrical signal output from the O/E converter is the original signal, which passes through the disclosed Reshaping/Limiting stage before entering the identification unit. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that, given the reshaping function inherent to the decision circuit of the Retiming block of Mokhtari et al., the separate Reshaping/Limiting block as disclosed could be removed as being redundant depending on the degree of distortion of the incoming signal, since the Retiming block both reshapes and retimes. In the case where the Retiming block performs all reshaping and retiming functions, the original output signal from the O/E converter would go directing to the Retiming block. Mokhtari et al. do not disclose deriving a bit rate of the original signal directly from a voltage level of the low-pass filtered signal without using a phase locked loop. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Banwell et al. with Mokhtari et al. as described above for claim 17. The combination of Mokhtari et al. and Banwell et al. disclose the low-pass filter and bit rate deriving circuits that follow the compare circuit (Mokhtari et al.: fig. 3 and Banwell et al.: fig. 3), but do not disclose an analog-to-digital converter. Ishihara discloses a bit rate deriving circuit that has an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal (fig. 23 and col. 15, lines 38-59). It would have been obvious to an artisan at the time of the invention to include the analog-to-digital converter, as taught by Ishihara, after the filter in the combination of Mokhtari et al. and Banwell et al. (Banwell et al.: fig. 12a), to digitize the filter output, providing the advantage of quantizing the voltage level to specific value by converting to digital.

Regarding claim 2, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses an apparatus comprising an optical receiver for receiving optical signals having a plurality of different bit rates (Mokhtari et al.: page 508, col. 1, paragraphs 3 and 4).

Regarding claim 3, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses that the bit rate of the input optical signal comprises a transmission rate (Mokhtari et al.: page 508, paragraphs 1, 3 and 4).

Regarding claim 4, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses an amplifier for amplifying the original electrical signal received from the converter (Mokhtari et al.: page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1).

Regarding claim 5, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses that the amplifier outputs the amplified electrical signal to the identification unit (Mokhtari et al.: page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1; and fig. 1, fig. 3 and fig. 5).

Regarding claim 6, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses an apparatus, comprising: a fiber optic system including electrical 3R regeneration (Mokhtari et al.: page 508, col. 1, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes an optoelectric converter to convert an input optical signal to an original electrical signal (Mokhtari et al.: page 508, col. 2, paragraph 4).

Regarding claim 7, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses an identification unit comprising a bit rate identification unit (Mokhtari et al.: fig. 3 and 5, and page 509, col. 2, paragraph 1).

Regarding claim 8, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses that the comparing performed by the identification unit comprises the identification unit

performing an exclusive-OR logic operation upon the first and second signals (Mokhtari et al.: fig. 5).

Regarding claim 12, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses said first unit comprising a bit rate identification signal generator (Mokhtari et al.: fig. 3 and Banwell et al.: fig. 3).

Regarding claim 13, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses said second unit comprising a bit rate deriving unit (Mokhtari et al.: fig. 3 and Banwell et al.: fig. 3).

Regarding claim 34, the combination of Mokhtari et al. and Banwell et al. disclose a second unit comprising: a low-pass filter for filtering the signal output from the compare circuit, and determiner determining the bit rate in dependence upon the signal received from the filter (Mokhtari et al.: fig. 3 and Banwell et al.: fig. 3), but do not disclose an analog-to-digital converter. Ishihara discloses a determining circuit that has an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal (fig. 23 and col. 15, lines 38-59). It would have been obvious to an artisan at the time of the invention to include the analog-to-digital converter, as taught by Ishihara, after the filter in the combination of Mokhtari et al. and Banwell et al., to digitize the filter output, providing the advantage of quantizing the voltage level to specific value by converting to digital.

Regarding claim 41, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses that the recovery unit comprises a programmable recovery unit (Mokhtari et al.: fig. 3, where the variable-rate recovered clock, considering the applied teaching of Banwell et al. fig. 3, input to the decision circuit, makes the decision circuit a programmable recovery unit).

5. Claims 26 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. in view of Banwell et al. as applied to claims 17, 19-25, 28, 30-32, 42 and 43 above, and further in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claim 26, the combination of Mokhtari et al. and Banwell et al. discloses a method, as described above, comprising: receiving an optical signal original signal using an optoelectric converter, converting the optic signal to an electrical signal, forming two duplicate signals and delaying one of the signals by a predetermined quantity of time. Mokhtari et al. do not disclose that the two duplicate signals are output from a buffer. Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., prior to splitting the signals for the compare circuit, in order to raise the two split signals to the optimal levels for sending the signals to the compare circuit.

Regarding claim 35, the combination of Mokhtari et al. and Banwell et al. discloses two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals comprising a primary signal and a secondary signal (Mokhtari et al.: fig. 5); a delay unit for receiving the primary signal, for delaying the primary signal by the predetermined quantity of time, and for outputting the primary signal, the delayed primary signal comprising the first signal and the secondary signal comprising the second signal (Mokhtari et al.: fig. 5); and an operator unit for performing the exclusive-OR logic operation upon the first and second signals (Mokhtari et al.: fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit for receiving the original electrical signal and for outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose an input buffer amplifier amplifying the original electrical signal and

outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., prior to splitting the signals for the compare circuit, in order to raise the two split signals to the optimal levels for sending the signals to the compare circuit.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. in view of Banwell et al. and further in view of Ishihara, as applied to claims 1-8, 12-13, 34 and 41 above, and further in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claim 15, the combination of Mokhtari et al., Banwell et al. and Ishihara discloses two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals comprising a primary signal and a secondary signal (Mokhtari et al.: fig. 5); a delay unit for receiving the primary signal, for delaying the primary signal by the predetermined quantity of time, and for outputting the primary signal, the delayed primary signal comprising the first signal and the secondary signal comprising the second signal (Mokhtari et al.: fig. 5); and an operator unit for performing the exclusive-OR logic operation upon the first and second signals (Mokhtari et al.: fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit for receiving the original electrical signal and for outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose an input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., prior to splitting the signals for the compare circuit, in order to raise the two split signals to the optimal levels for sending the signals to the compare circuit.

Allowable Subject Matter

7. Claims 16, 27 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to deriving a bit rate directly from a voltage level of a low-pass filtered signal without using a phase-locked loop have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's addition arguments, which are repetitions of applicant's previous arguments, have previously been fully considered and were found to be not persuasive. Detailed responses to applicant's previous arguments are already part of the record and not repeated here.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

11. Any inquiry concerning this communication from the examiner should be directed to N. Curs whose telephone number is (571) 272-3028. The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (800) 786-9199.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGUSTIN BELLO
PRIMARY EXAMINER